Testing and Verification Waveforms of a Small DRSSTC

Part 1

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6/24/2009

Power electronics, unlike other areas of electronics, can be extremely critical of small details, since the results can be expensive and dangerous. There are plenty of "gotcha's" that only become well understood with experience in the field. For the last 6 years, Solid State Tesla Coils have been a hobby of mine; they have a strong relationship with the power electronics field and have thus shaped my career. Within this paper I will address a couple of issues with building a Double Resonant Solid State Tesla Coil, particularly the testing and verification methods I use with my "universal driver" on a typical small-size DRSSTC.

In this paper I will NOT address: coil design or tuning. I will highlight some of the quirks dealing with my Universal Driver (UD) and some possible improvements that could be made. This paper assumes your DRSSTC is built up to at least the point of getting it to oscillate on its own feedback.

The Test Setup

After your coil is constructed (or at least done to the point of being functional) it's important to give the electronics a good testing to avoid possible failures later. You will require the following test equipment:

- 2-channel oscilloscope
- 2 voltage probes for the scope
- High-bandwidth current transformer*
- Variac
- Isolation Transformer for powering the bridge electronics

*I plan to release a paper about the construction of high-bandwidth CTs.

The isolation transformer is required not only for safety but so that you can attach scope ground (which is mains ground) to the power electronics (which are normally at mains voltage) without causing a short circuit. My isolation transformer has 2 primary windings and 2 secondary windings (though primary and secondary are relative terms, I can easily apply power to the secondary and extract power from the primary). This transformer allows for various step-up/down ratios, but I wire it for a 1:1 ratio. If you can't find a true isolation transformer like this, pretty much any other transformer that will give you at least 50VAC and a few amps of current will suffice for basic testing. I prefer to have the ability to run full voltage into my electronics while isolated so I can view waveforms at full operating condition.

2kVA isolation transformer

The next important bit of equipment is the oscilloscope. I use a small DSO (digital storage scope) but you can get by with far less. Id suggest having at least 20MHz bandwidth, and a good set of 10:1 voltage probes so that you can view 200-400V signals safely.

A trick that helps avoid false noise on your signals is to use common mode chokes on the voltage probe and even on the AC power cable for the scope. I happened to have some large ferrite toroids that I could wind the cable through (seen in the picture below). Common mode noise is typically generated by fast changing voltage signals, and occurs because of the capacitance between the scope (which is grounded to the line, thus allowing for HF ground loop noise) and the high frequency source of noise (the bridge). Common mode inductors impede the flow of this noise, but since the inductance is common to both the signal and return lines on the scope probe, it does not slow down the desired differential signal being measured by the probe. The filters will help avoid common-mode noise from turning into differential mode noise (or signal presented on the scope). Clamp-on ferrite beads would also be a good choice. You can operate without the filters completely, but you may get waveforms that look noisier than they really are, particularly near the voltage transitions on the output of the bridge circuit.

TDS210 with Common-Mode filters

Test Setup
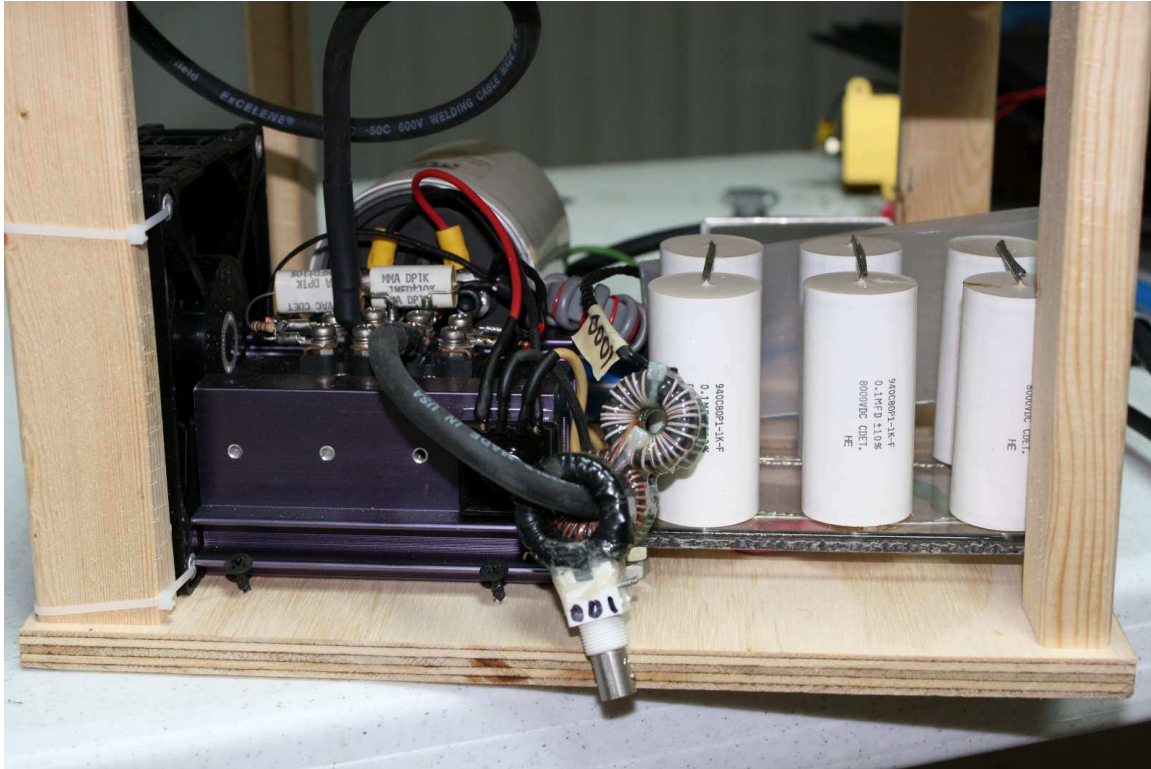
DRSSTC bridge and home made CT

**Verifying the Driver Board Output:**

Ok, so on with the testing. The first thing I check is if the driver board outputs a pulse from the gate drive section when a light pulse is received by the fiber optic Rx. With the GDT wired into the output and a lack of input signal to the driver, the waveform is ugly indeed:
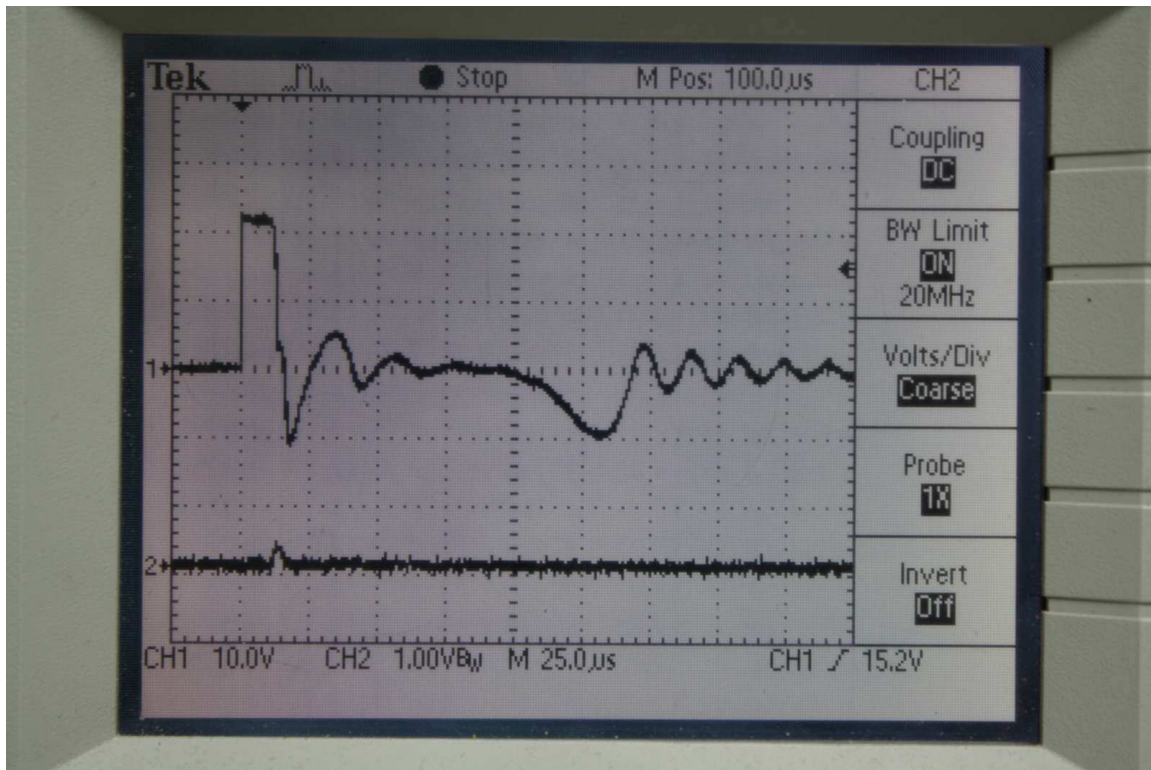
What you are seeing (on channel 1) is caused by pulsing the GDT primary so long that the core has saturated and excited various parasitic effects of the circuit. The pulse is generated by the pulse width provided by the interrupter plus a syncing window provided within the driver circuitry itself, in this case its about 100uS total. Initially there is a crisp square signal applied to the primary for about 15uS, at which point the GDT saturates and the leakage inductance rings with the 10-20uF of DC blocking capacitance (down to 0V). Ringing is quickly damped by the 10 ohm resistor in parallel with the DC blocking cap, and at this time there is 24V across the 10 ohm resistor, implying about 2.4A of current flow! Luckily the duty cycle is very low. After about 100uS you can see some more action as the driver output returns to its OFF state, again exciting a resonance with the GDT and series DC blocking cap. Channel 2 shows the other side of the gate drive, not much action here, and this is correct.

NOTE: I suggest one avoids operating in this state for any prolonged period of time, particularly at high pulse rates. Not only does it beat up on the 10 ohm damping resistor, but it causes particularly large surge currents to flow through the driver MOSFETs. This is an unfortunate event that this simple driver can't avoid for now. This has not been a problem for most of my coils, but others have reported MOSFET output failures.

Under proper operating conditions (with either feedback or signal generator feeding the input of the driver), the 2 gate driver outputs should look like the following complementary square signals:
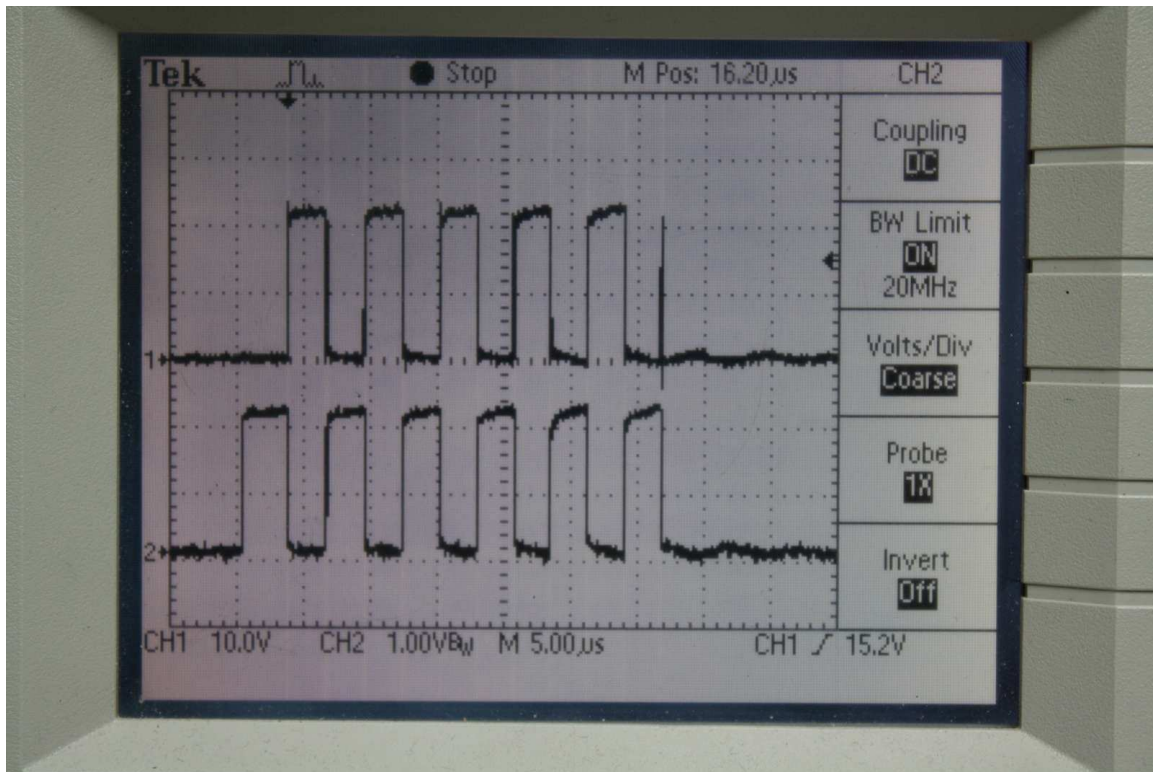
Notice on channel 1, at the very end there is an ever so short "glitch". This occurs because the driver is disabled by a transition in the feedback signal. But, the feedback signal gets to the gate drivers before the flip flop can shut them off, so you see the start of one more cycle just as the flip flop turns the gate driver off. This little glitch can indeed show up on the secondary side of the GDT, and it looks like this:
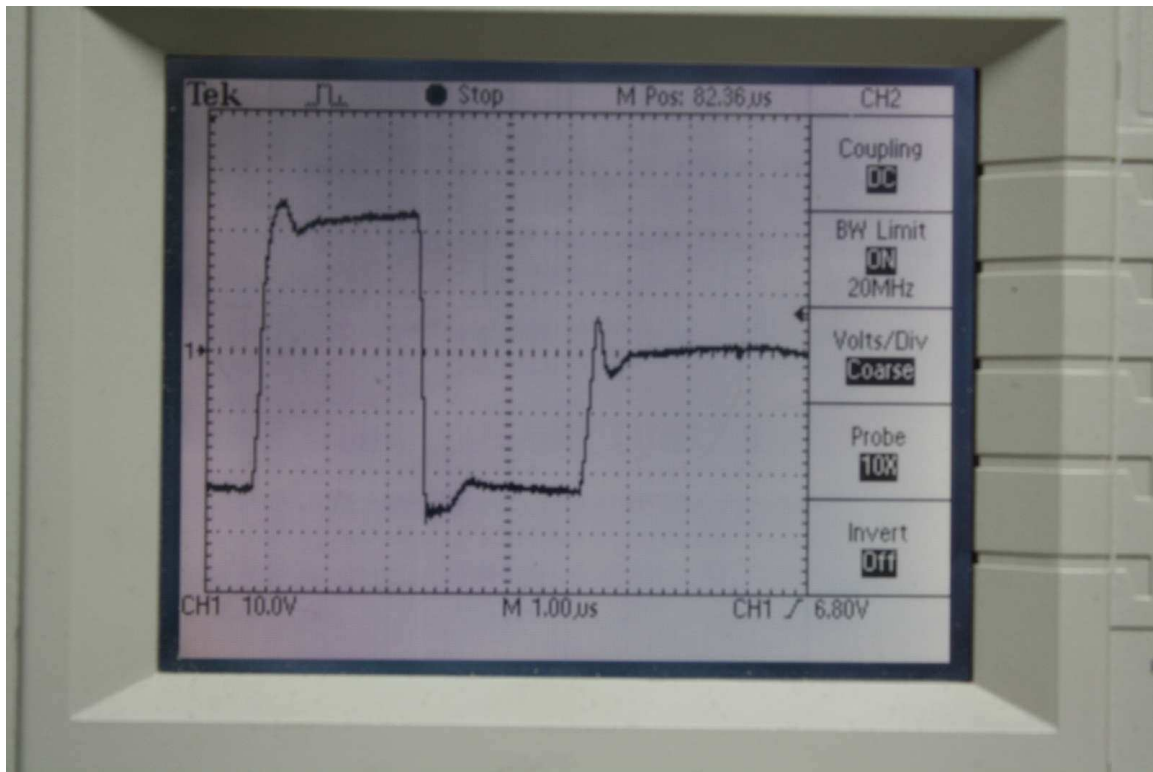
Secondary side switching glitch
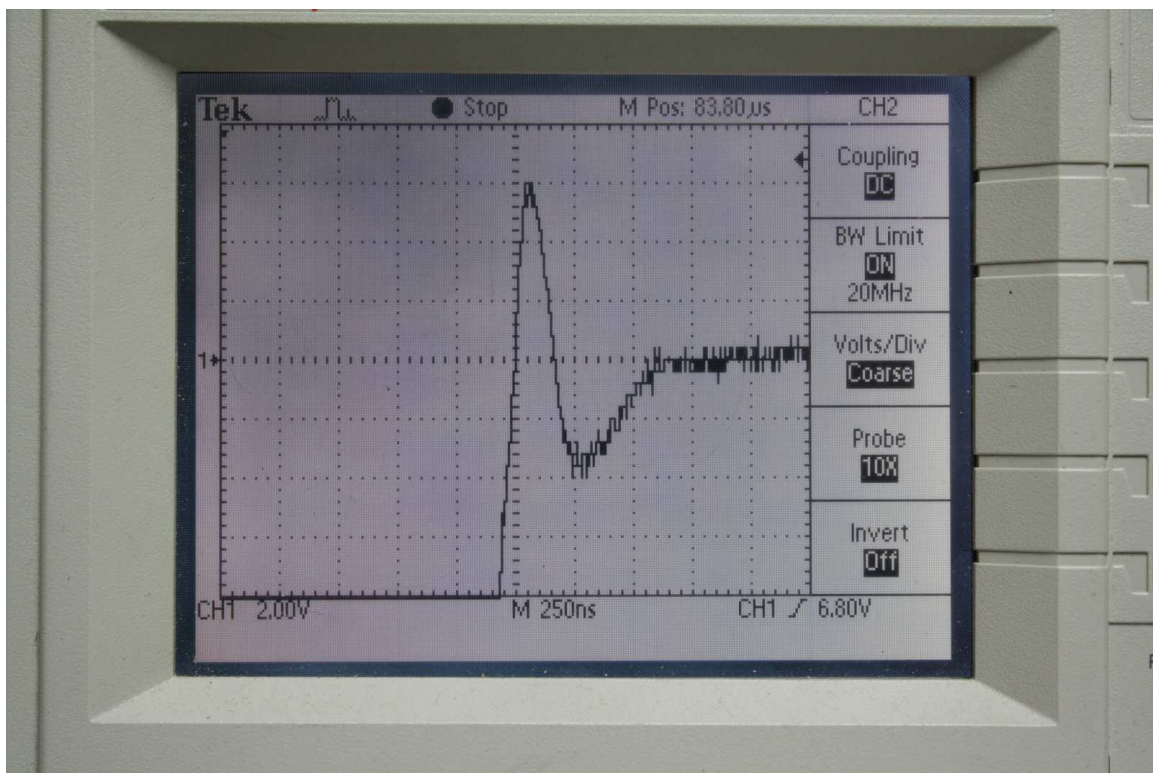
Zoomed in on switching glitch, Vpk = 6V, T = 200nS

This glitch is mostly harmless, if it does manage to turn the IGBT ON, it only adds a bit more switching losses. The risk of it turning a device ON can be reduced by increasing the series gate resistance. As far as I know, there is no good fix for this problem, you could delay the signal to the gate drive so that the flip flop has time to disable before the next switch event, but adding any more delays is not good.

GDT Secondary Waveforms

With the system oscillating, it's a good idea to check out each of the waveforms from G to E on each IGBT. Warning, do not mistakenly probe 2 IGBTs in a half-bridge at once! The grounding clips on the probes will short out the bridge!

I like to use a series gate resistor bypassed with a 100V 1A schottkey diode (MBR1100). Determining the gate resistance is for another paper… but it explains the waveforms shown below.
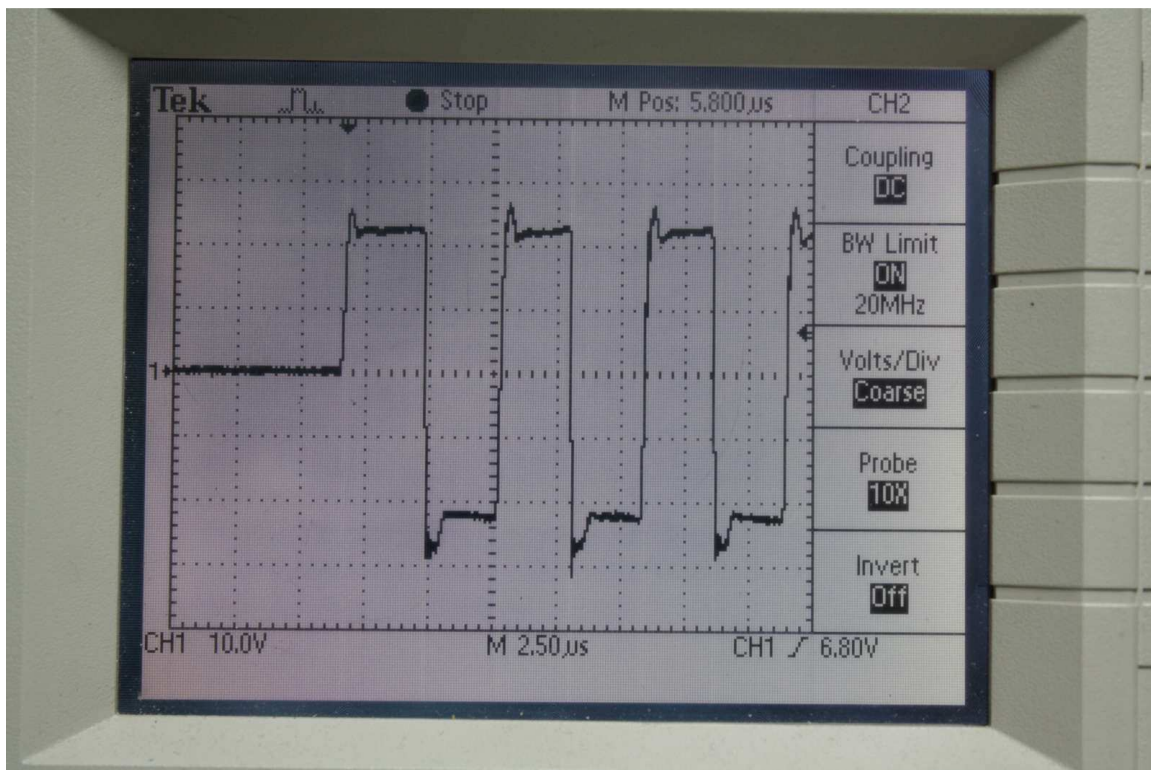

Typical Vge waveform

Seen here is a fairly typical waveform present at the Gate and Emitter terminals of the IGBT. There is a small overshoot on the rising/falling edges, and its worse on the falling edge because the current is higher (no series gate R, bypassed by diode). You should also, note upon closer inspection, that the rise time is significantly slower than the fall time due to the resistor/diode pair; this buys you some dead-time where both IGBTs are OFF.

Primary B-field playing with the scope!

The above scope shot highlights a very important issue. There are very large, high-frequency currents flowing in the primary circuit, and thus any loop of wire suddenly becomes an antenna with a voltage induced by the dB/dt (change in flux over change in time). This can give the impression of "sagging" or "ringing" waveforms, it just so happens the sagging/ringing is at the natural Fo of the primary system! This is caused by voltage induced magnetically, into your scope probe wiring! The fix is to try and squeeze down the loop area of the probe tip and the ground clip, preferably by twisting the ground clip around the probe body itself:
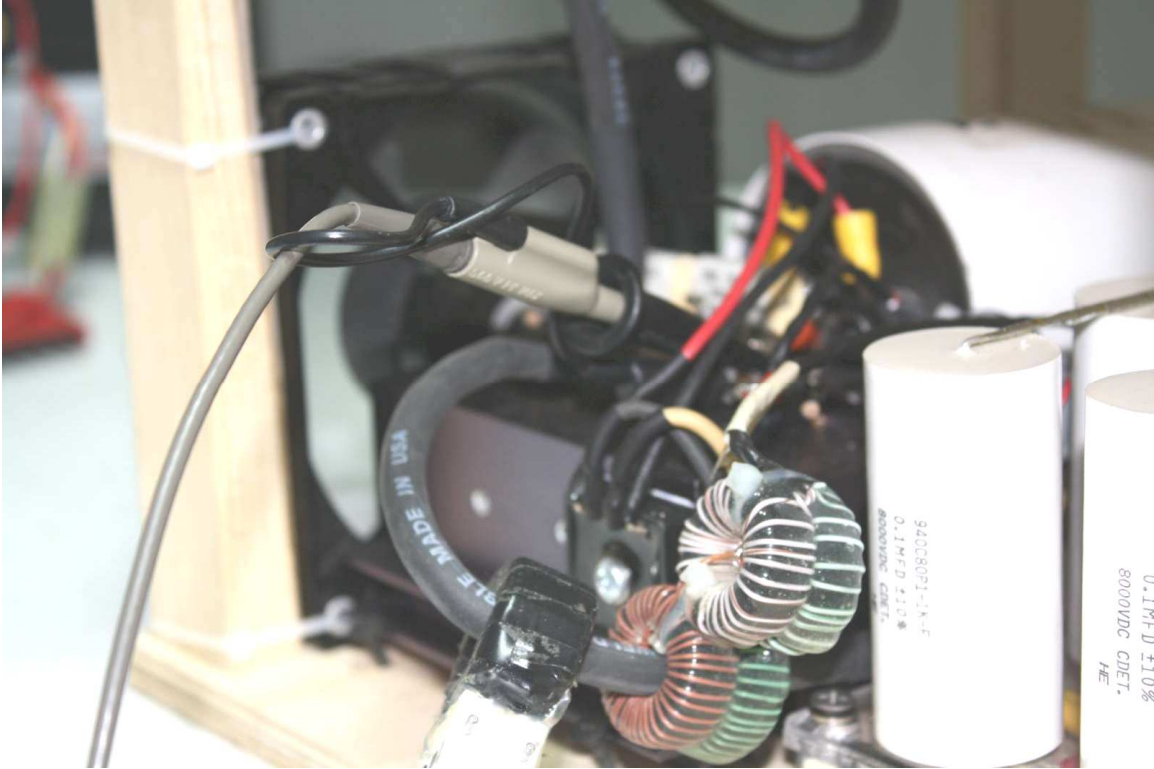
Squeeze down the probe signal loop!

The resulting waveform was then captured:
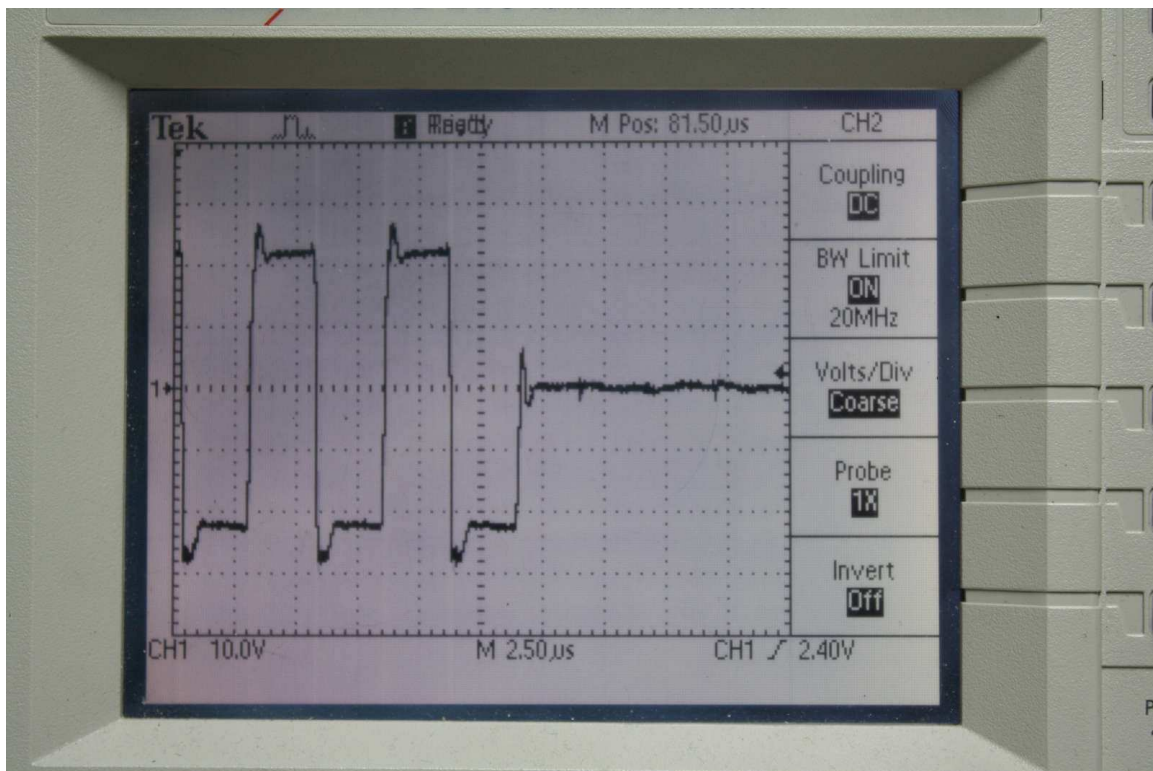
Same GDT waveform after squeezing down the loop: no drooping/ringing!

What qualifies as "satisfactory" for a Vge waveform? Well, there should be no overshoot greater than say 30Vpk. There should be no significant "ringing" or "glitches" at the rising/falling edges, though this will show up to some degree (see below). The fall time should be as quick as possible (typically 100-200nS), and the rise time should not be excessively fast (often 2X the fall time). The ideal waveform is dependent on other conditions, so some experimentation is in order to identify the best gate resistance and acceptable levels of gate wiring inductance.

As the voltage is increased on the Vce of the IGBTs, the miller capacitance (or Ccg) begins to apply a "negative feedback" to the gate voltage. Effectively, as the IGBT tries to shut off, its Vce rises quickly, which couples a positive voltage back into the IGBT gate (it tries to turn itself back on). Normally this is not a problem with bipolar gate drivers (ones that have a negative drive bias) but it's something to watch out for. On Turn ON, the opposite situation occurs. A quickly falling Vce tries to turn off the gate. The waveforms below highlight some of the nastiness that can show up:
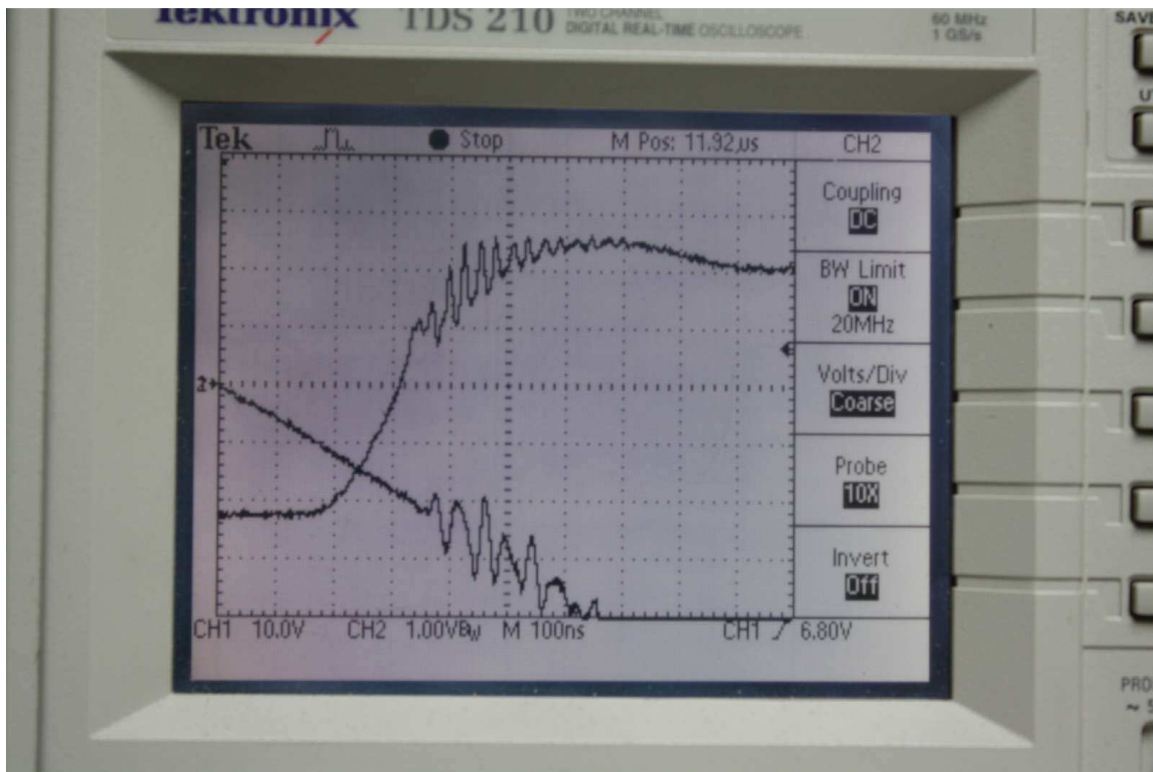

Miller effect along with diode recovery noise coupled to Vge

There are 2 traces here, the one sloping downward is the primary current (it shows that there is about 200nS between zero crossing and gate signal response). The other wave is the Vge. At about 10V on the screen, the IGBT turns ON hard, causing a forced recovery of its neighboring free-wheeling diode. This recovery causes significant ringing on the Vce, which is coupled to the Vge via miller capacitance. In this case the gate driver over-powers the miller feedback and there is nothing to worry about, it just looks ugly. Severe cases of this would show the Vge temporarily ringing down to 0V or less! Its worth mentioning that the noise may not in fact even be a real part of the Vge

waveform, since it also appears on the primary current waveform. This is part of the ambiguity that arises from scoping out power electronic circuits. The designer must know if certain levels of this noise are acceptable or not, and in this case if the noise is real it's still at an acceptable level.

Finally, I want to draw attention to what happens under weak feedback conditions. In the case of my small half-bridge coil, when operating at less than 35VDC, the feedback signal is weak and the system gain is not sufficient to provide a strong oscillation. The resulting waveform is captured:
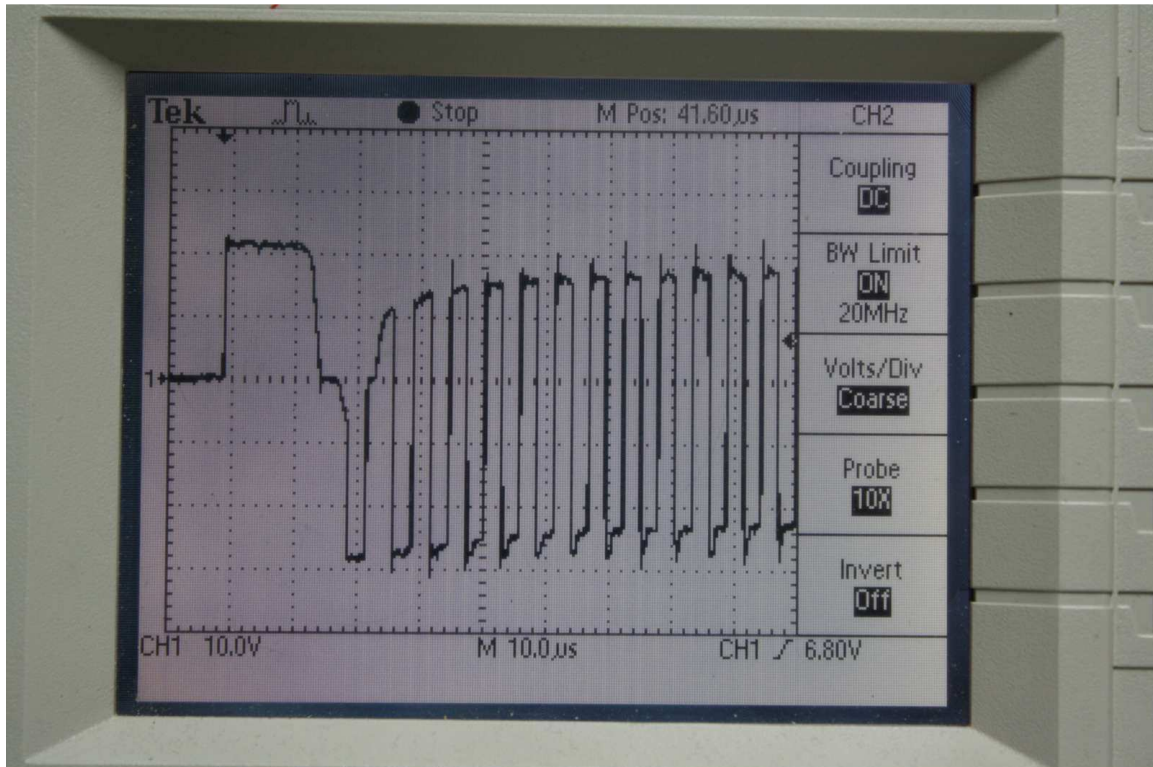

Vge under weak oscillation condition

You can see the gate gets a 12uS pulse, but oscillation does not start properly. Eventually after the GDT saturates, the primary is once again "pinged" but this time it does start up properly and oscillation resumes. This problem should only show up at very low voltages. A possible fix would be to decrease the turns ratio of the feedback CT so that it provides more current to the feedback input (thus providing a stronger voltage signal across the clamping diodes). In the case of my half-bridge, the problem is worsened by the possibility that the primary capacitor was left with a voltage such that the initial starting pulse from the GDT is not the correct polarity (it tries to charge the primary cap in the same voltage polarity it's ALREADY charged with!). In this case, an alternating pulse is required to start oscillation. In any case, just be sure the problem goes away as the input voltage gets past 50VDC or so. Below this level, IGBT damage is very difficult to achieve!

Bridge Switching Voltage

One of the most important things to observe is the "trajectory" of the Vce waveform. Because my driver switches the IGBTs just after the primary current zero crossing, this implies that the current is briefly conducted by the free-wheeling (a.k.a. anti-parallel or co-package) diodes. Soon, though, the IGBTs are switched ON and thus the diodes are "switched" OFF. This results in some switching loss and causes a voltage spike to appear across the diode that was just turned off due to energy stored in the bus inductance. This voltage rings with the bus L and the parasitic C across the IGBT/diode junctions, and typically shows up in the 10MHz region or higher.
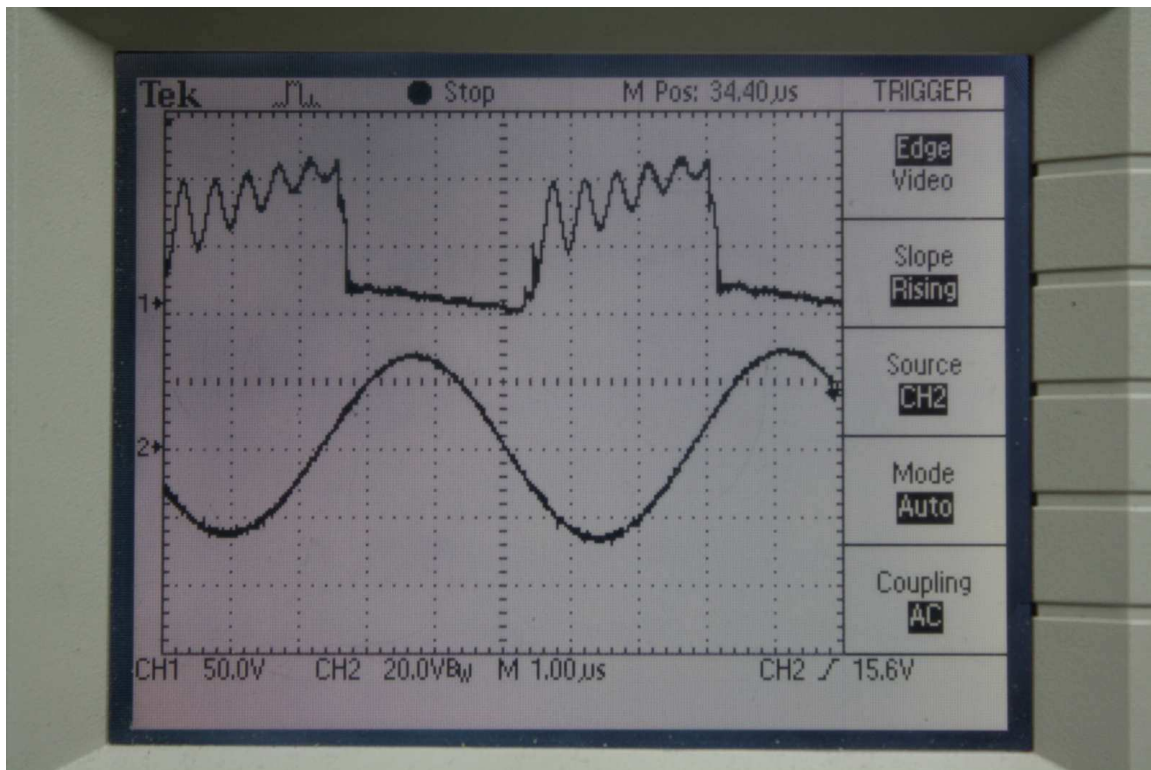
Half-bridge output voltage and primary current
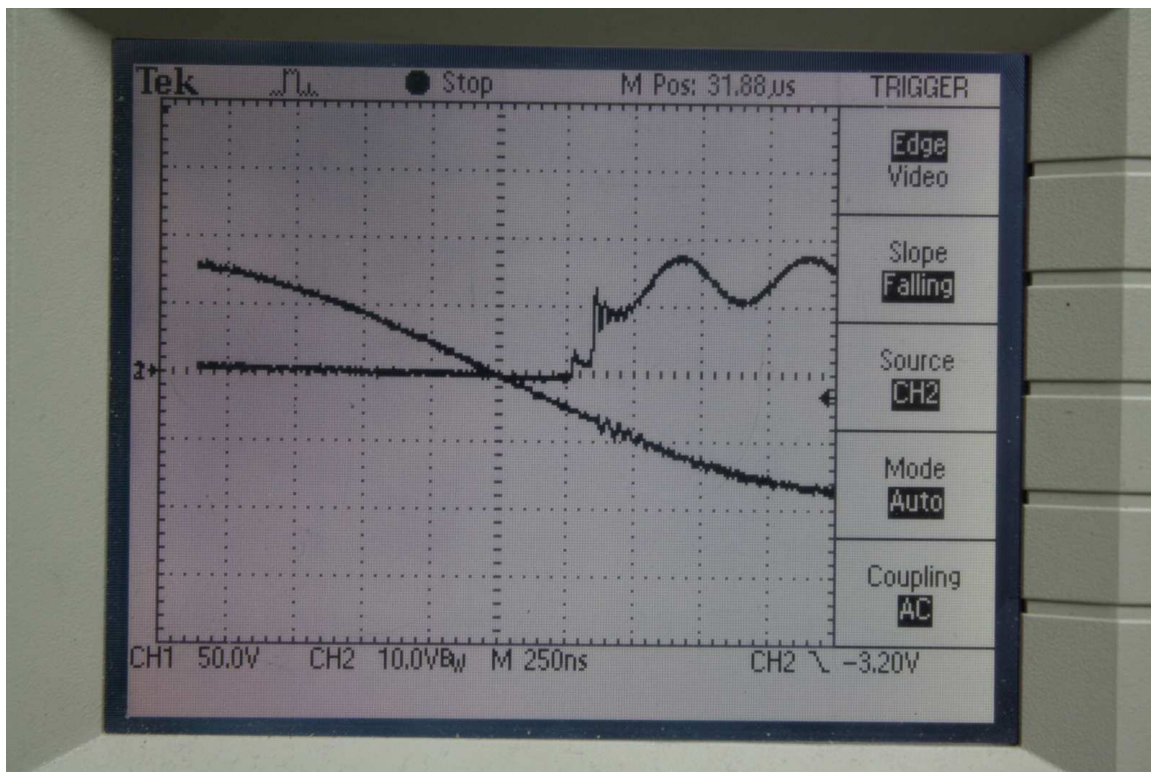
Zoom in on the IGBT turn OFF

Zoom in on the IGBT turn ON

As seen in the above 2 pictures, the actual delay time between primary current zero crossing and IGBT switching is around 250 to 350nS. You can see an initial "step" in voltage at the 250nS mark, this is indicative of the neighboring IGBT turning ON/OFF (in the order of the pictures shown respectively). There is a short dead-band of about 100nS where the Vce trajectory floats somewhere in the middle, and then at about 350nS, the IGBT turns OFF/ON and there is some MHz region ringing (albeit, quite small).

The long-term ringing on the top of the Vce waveform is caused by the bus inductance ringing with the snubber capacitance, its in the 100's of kHz range typically.

The following picture highlights the effects of bus inductance on the output Vce waveform:
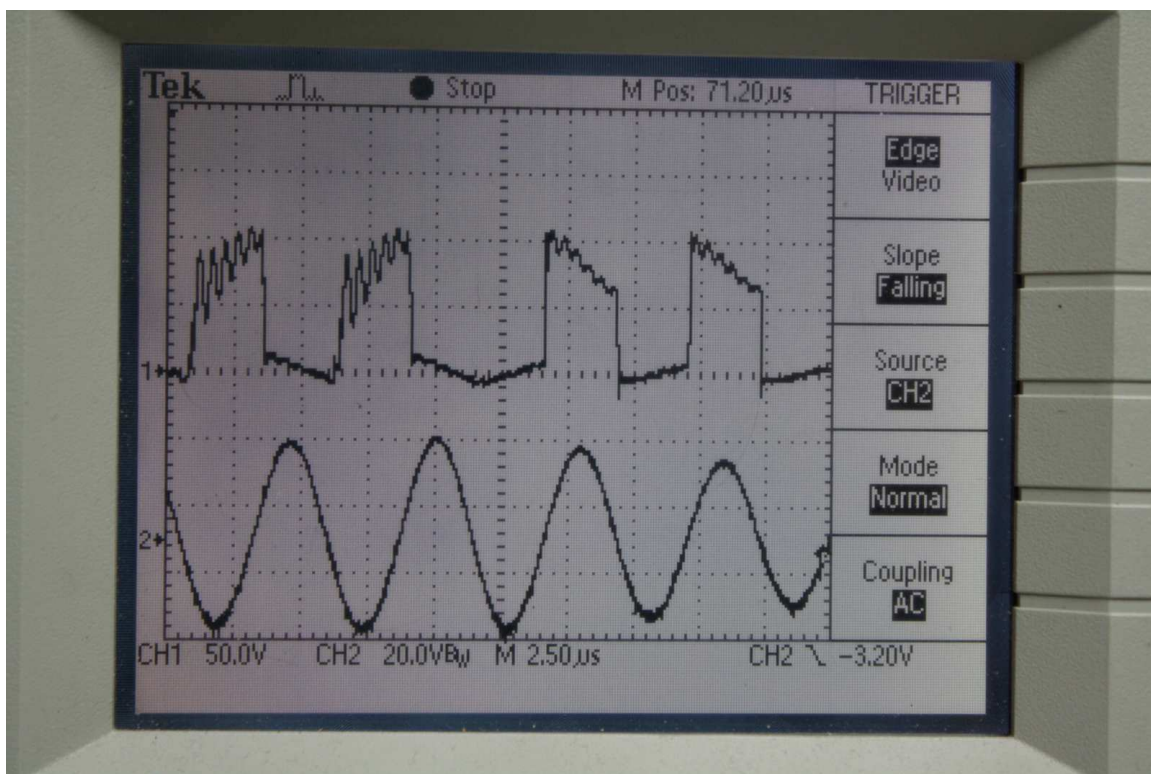
Effect on Lbus on Vce

You can no longer see the Mhz ringing (from C junction and L snubber). Its clear to see the ringing from Lbus and Csnubber, but there is also a very "low frequency" or "slope" to the Vce waveforms. Part of this is caused by magnetic pick up on the probe, but the rest of it is caused by Lbus*dI/dt (where I is the primary current). There is also some voltage swing caused by the ESR of the bus capacitors (the large lytics) but mostly this sloping is due to the inductance of the bus circuitry. This waveform also shows the transition between the tank circuit being a Load and a Source. As you can clearly see, the primary current begins to decay and the output voltage has reversed (this is because now the bridge is merely a full-wave rectifier for the energy left in the primary circuit).

I hope the preceding text and waveforms serve as an example of a properly working DRSSTC. As an engineer it's important to realize why things are not ideal, and what is acceptable for circuit performance.