Effects of Initial Conditions in a DRSSTC

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The DRSSTC is based on the idea that the initial conditions of the tank circuit are that the primary inductor has zero current flowing and that the primary capacitor has zero stored charge. The zero current is relatively easy to achieve, given enough time for the system to discharge, either via streamers removing all of the energy, or any excess energy being rectified back to the DC bus. The problem is the charge left on the capacitor, which is not necessarily zero, but could end up at any potential that is less than the bus voltage.
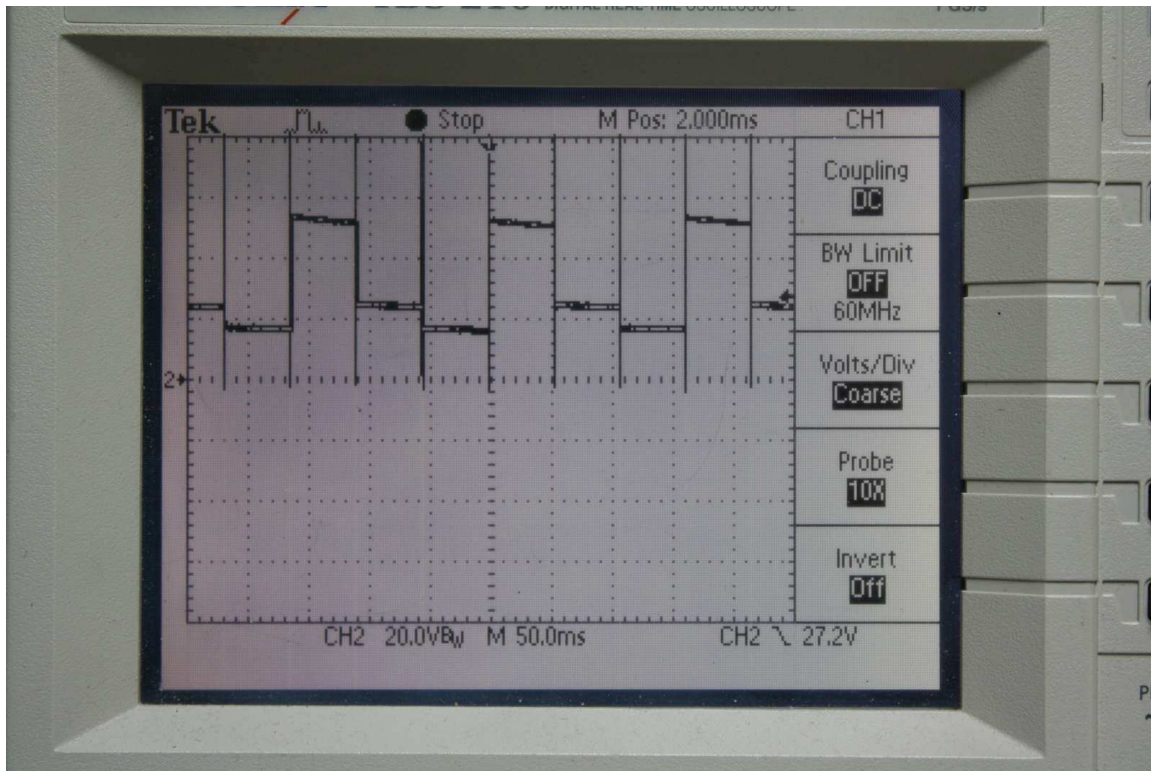
Trace showing the MMC residual voltage after each firing, note the time scale.

Why is this left-over charge a problem? In my system, oscillation is based purely on feedback from the primary current, without this feedback, the system cannot oscillate. The capacitor charge can either be a benefit, or a hindrance depending on the polarity of the charge with respect to the start-up voltage applied from the bridge. Lets say the capacitor is left with a +Vbus charge, and upon receiving start command from the controller, the bridge switches in such a manner as to apply +Vbus to the tank circuit. Because the capacitor is already charged to +Vbus, there will be no current flow from the bridge to the capacitor, which means there will be no primary current feedback to sustain system oscillation. This then causes the gate drive system to fall on its face as the GDT saturates from exceeding its Volt-Second product. Interestingly, as the GDT saturates, the leakage inductance "rings" such that some voltage is applied to the opposing bridge switches (which were initially given an OFF command) causing the system to spring to life! This is a sloppy, marginally stable situation that needs to be fixed.

The waveform below shows this phenomenon on a small half-bridge driven system, where the tank capacitor is left with zero charge in this case, where the driver tends to drive the capacitor to zero charge upon start up:
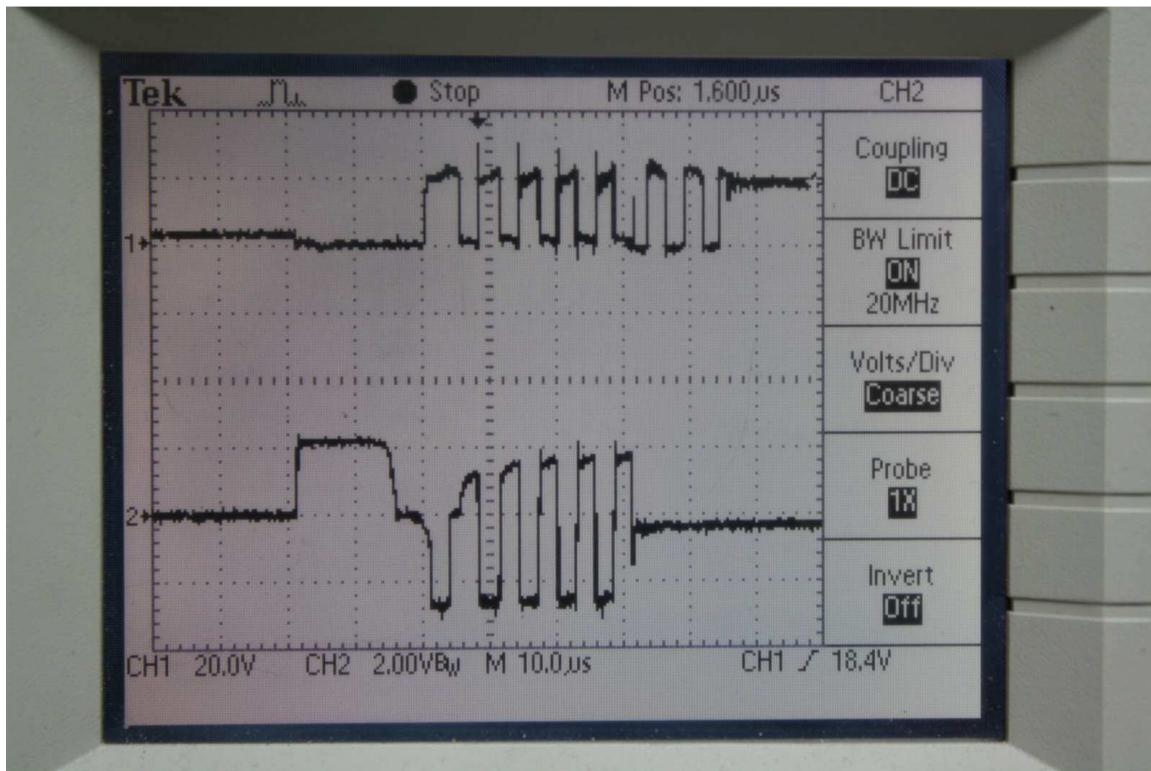
Half-bridge output and GDT output voltage during a false start

Trace 1 shows the half-bridge output voltage, and since the tank circuit is returned back to the bus negative rail (which is also the reference for my scope probe) you are actually seeing the tank capacitor voltage while the system is not oscillating. So at the start the tank cap is nearly discharged (this was done intentionally with a bleeder resistor). Trace 2 shows the Vge for the low-side IGBT. Upon start up, the driver switches the low side IGBT ON, which of course only serves to try and further discharge a mostly discharged tank capacitor, in which case the current flow in the primary circuit is so small that it does not yield enough signal strength for oscillation. As the gate drive output collapses, it somehow manages to turn on the high-side IGBT, which charges the output to Vbus, and causes current to flow into the primary circuit, giving feedback and causing solidly sustainable oscillation. Note a problem here… the saturated GDT has a volt-second imbalance, which is seen here by a slowly rising positive gate drive waveform (it takes about 3 cycles for it to return to its normal bias point). The negative portion of the gate drive waveform is clipped hard with TVS diodes; otherwise it would show an excessively negative waveform here. The TVS clamping diodes help reset the core to its natural V-s balance, without them the IGBT gates could see as much as 48V peak, or the total peak-to-peak applied voltage, but in one direction! This is good reason to always use some form of gate voltage clamp protection.
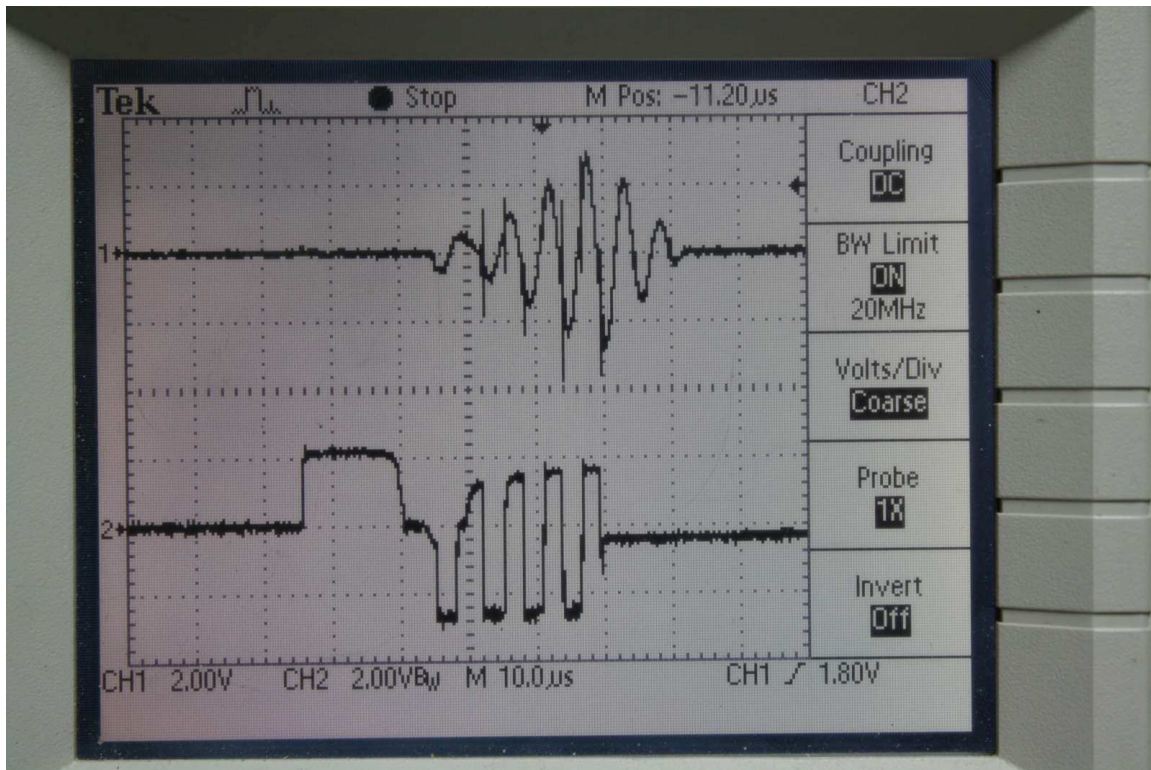
Primary current vs. Vgs under false-start condition

In this waveform, trace 1 is the primary current, which as seen is basically zero during the false start pulse. This false start condition is somewhat saved by the fact that the primary current is very low at start up, and the system can put up with poor gate drive waveforms and such because its not switching appreciable currents yet. But, this condition should be avoided when possible!

For most systems, this condition will naturally desist as the bus voltage is increased, because the capacitor will not typically remain charged at the full bus voltage, and even if it is close, it's usually enough difference from the applied bus voltage that enough current flows to kick-start the system normally.

So what can be done to avoid this issue?

BLEEDER RESISTORS: If you are running a full-bridge system, you could use a bleeder resistor tied across the bridge outputs which will naturally try to discharge the tank capacitor after each firing. Why not put the resistor straight across the capacitor? Well then it would see many kV of RF, which requires a high voltage resistor. Putting it across the bridge outputs means that it never sees more than Vbus (plus some transients), and it still functions effectively during the "down time" of the inverter. Something on the order of 10 kilo ohms should be sufficient for most coils, I believe. Make sure to rate the power dissipation for worst case, full bus voltage applied across the resistor continuously (12.5W for 350VDC, or 50W for 700VDC).

If running a half-bridge system, you have to be a little more careful about how your system is set up. You can return the primary coil to either the positive or negative

bus (assuming a single bus capacitor) or you can return it to the center point of 2 series bus capacitors (Vbus/2). In my case I returned the primary to the negative bus rail. Given that the polarity of my gate drive signals is such that the low-side switch is turned on first, this is an unfortunate choice! The fix in this case would be to use a "pull up" resistor on the bridge output to help sway the tank capacitor to have some positive voltage upon start up, which would naturally aid in starting oscillations.

The best setup for a half-bridge would be to have a split-rail supply (2 series lytics, perhaps in voltage doubler arrangement), in which case you would have a bleeder resistor tied between the half-bridge output and this center point. You would of course return the primary to the center point as well.

As an example with a 0.5uF tank capacitance, the time constant is about 5mS, which means the tank capacitor should be fairly close to zero charge between firings at 200hz. I'm not sure if it's worth going more aggressive on this issue, such as a manual reset of the capacitor voltage (some sort of extra switch). I personally have not noticed this initial condition problem when the bus voltage was more than 25% of the maximum intended operating voltage.

INCREASE SYSTEM GAIN: The problem could also be reduced by increasing the gain of the feedback signal. You might normally think this means using a higher turns-ratio on the current transformers, but this would actually be a step in the wrong direction. The reason is that the CT is loaded with diodes, which have a tiny amount of capacitance across their junctions. The CT is loaded capacitively until its producing enough current to overcome this and bias the diodes ON. To get more signal across the capacitor you have to supply more current from the CT, which means a lower winding ratio. The trade-off is that now you will dissipate more power in the clamping circuitry, I suggest one calculates the power dissipation in the zener diodes (its' roughly = 5V * Ict * duty cycle) before going to very low CT winding ratios.

The rest of the fix…

Now that the tank capacitor will naturally bias itself to a known state, there is one minor fix required on the driver board to make sure that the start-up drive signal is always the same. To improve system sensitivity, the feedback CT output was AC coupled into the 7414 inverter gate. This can present a problem caused by the hysteresis of this chip. Depending on how the voltage on that pin settles out from the previous firing event, it may alter the default level of the feedback signal. The fix here is simple, either don't AC couple the signal in, or put a pull down resistor on the 7414 pin 1. I opted to add a 100k SMD pull-down resistor to the nearby ground plane on my board. This reduced the input sensitivity since now there is a natural DC bias towards 0V, which makes start up slightly more difficult.
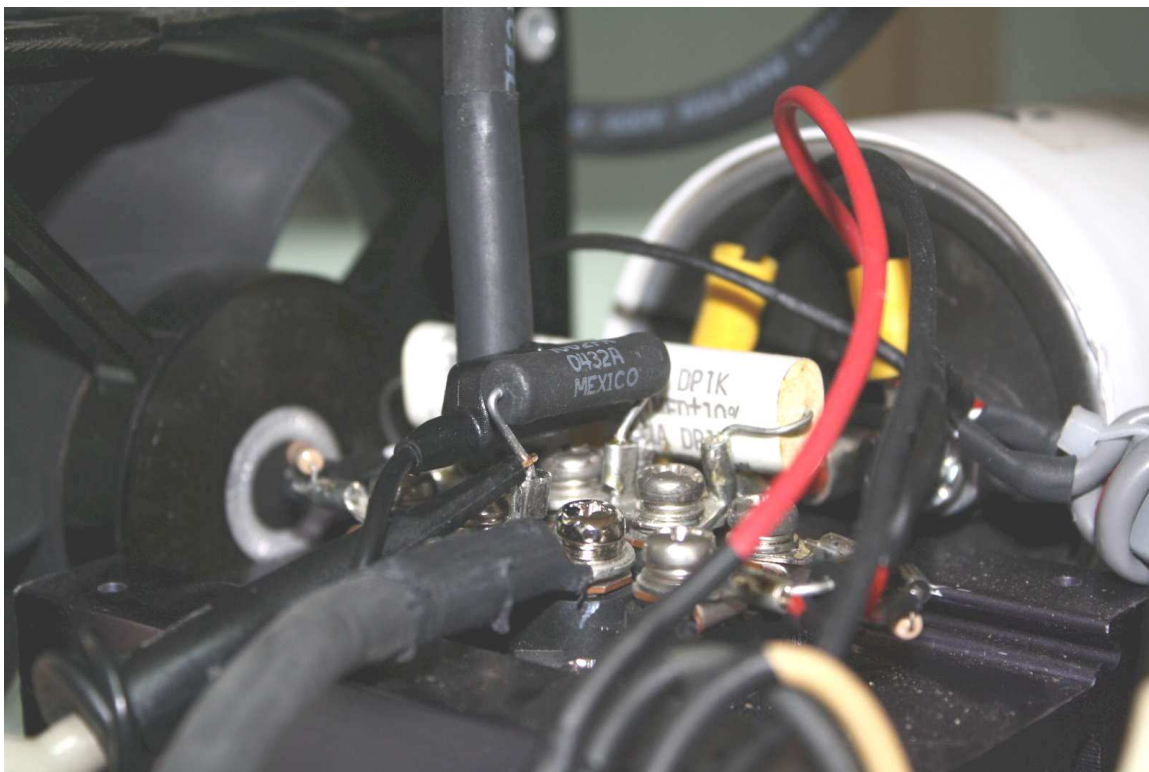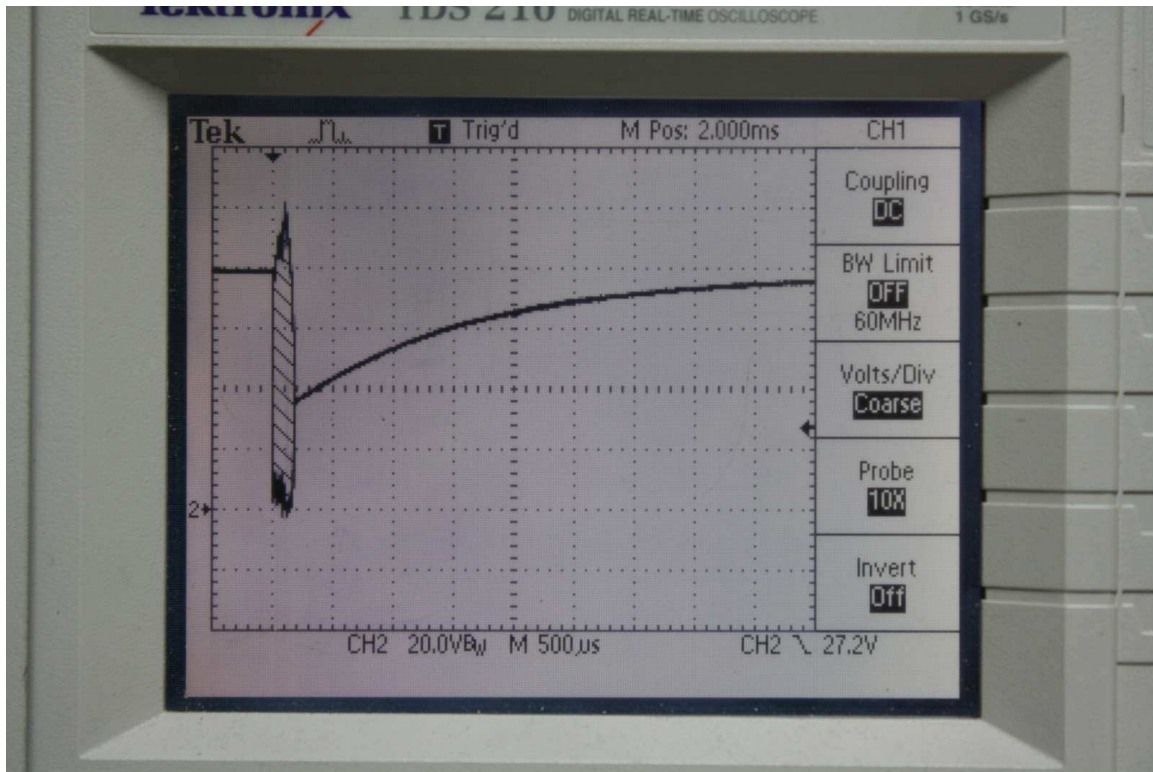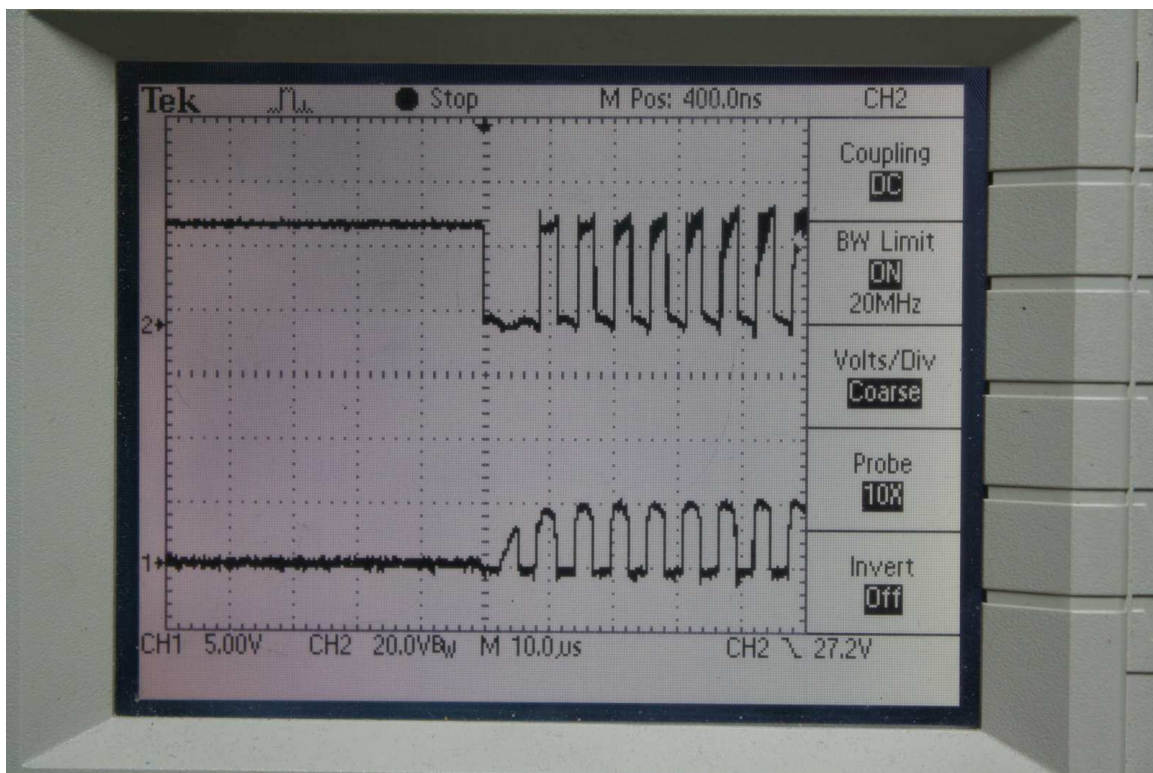
10k ohm resistor added from bridge output to DC+ rail
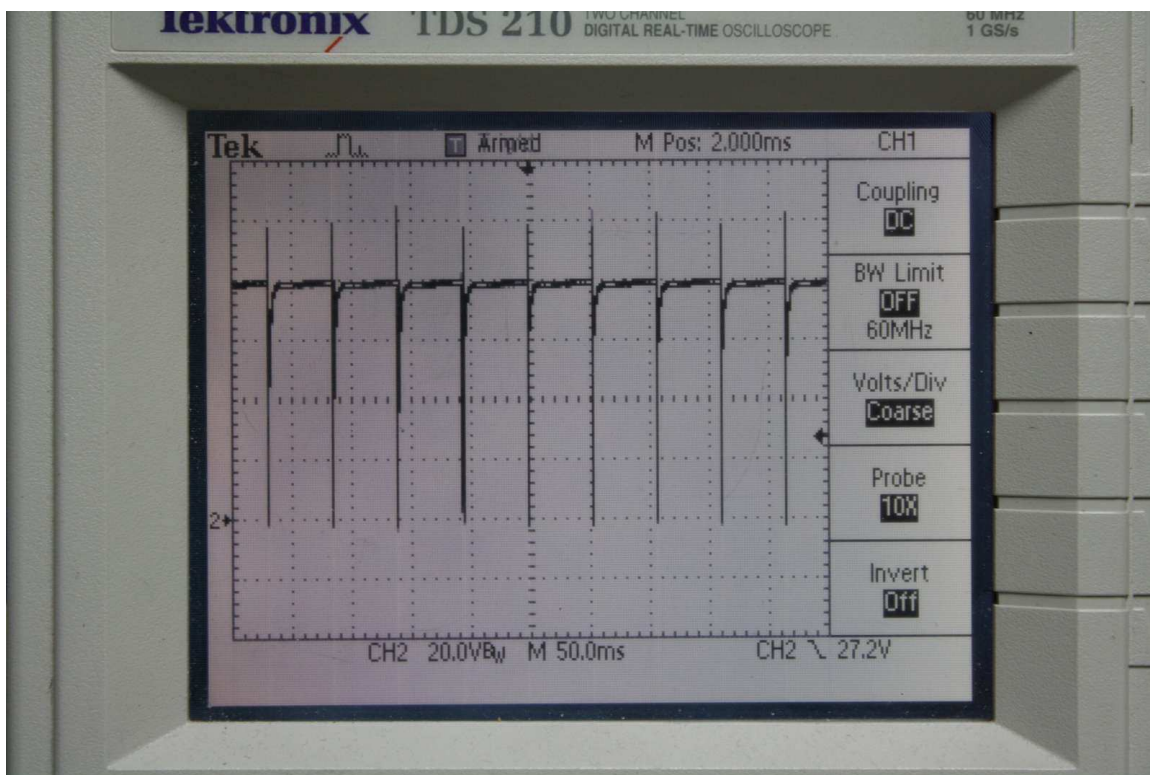
Capacitor residual voltage is now "fixed" with the addition of pull-up resistor, again note the time scale showing several firing events. Vbus = 80VDC.
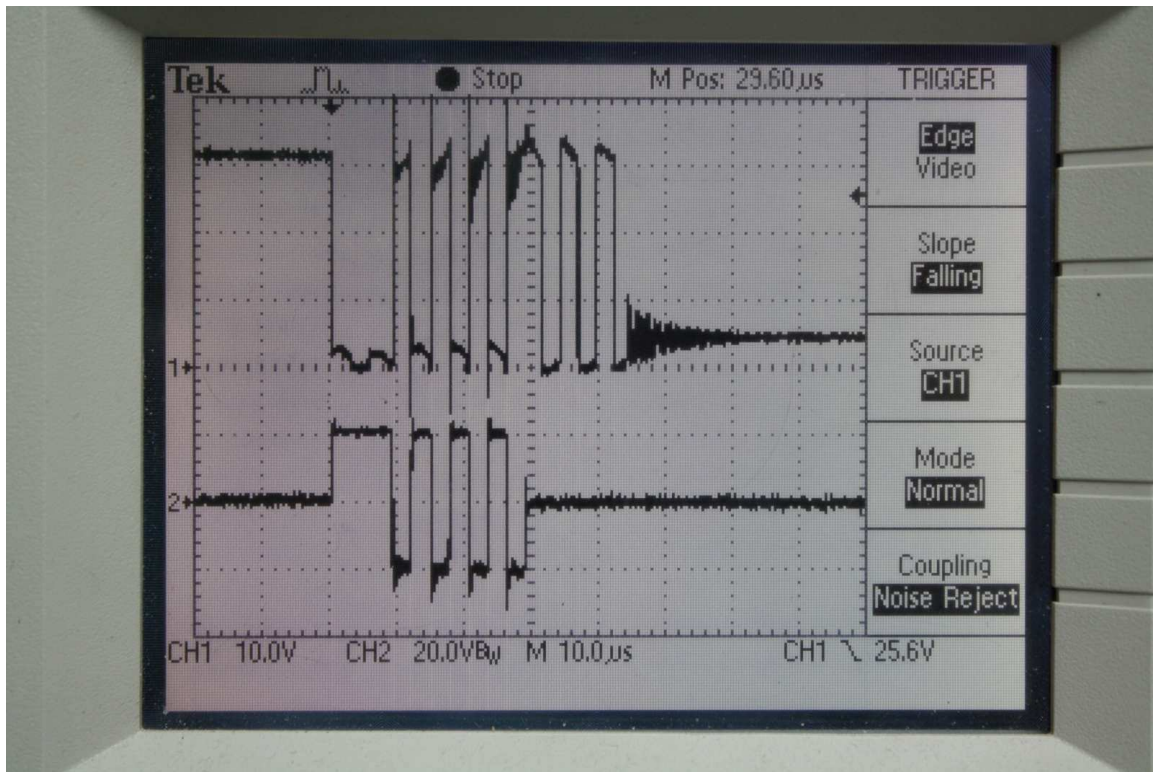
One bang with resistive recharge of the capacitor afterward

Top trace is output voltage from half-bridge, bottom trace is feedback voltage into pin 1 of 7414, the signal just isn't strong enough at the start so 1 cycle is missed. Note Vbus is only about 25VDC.
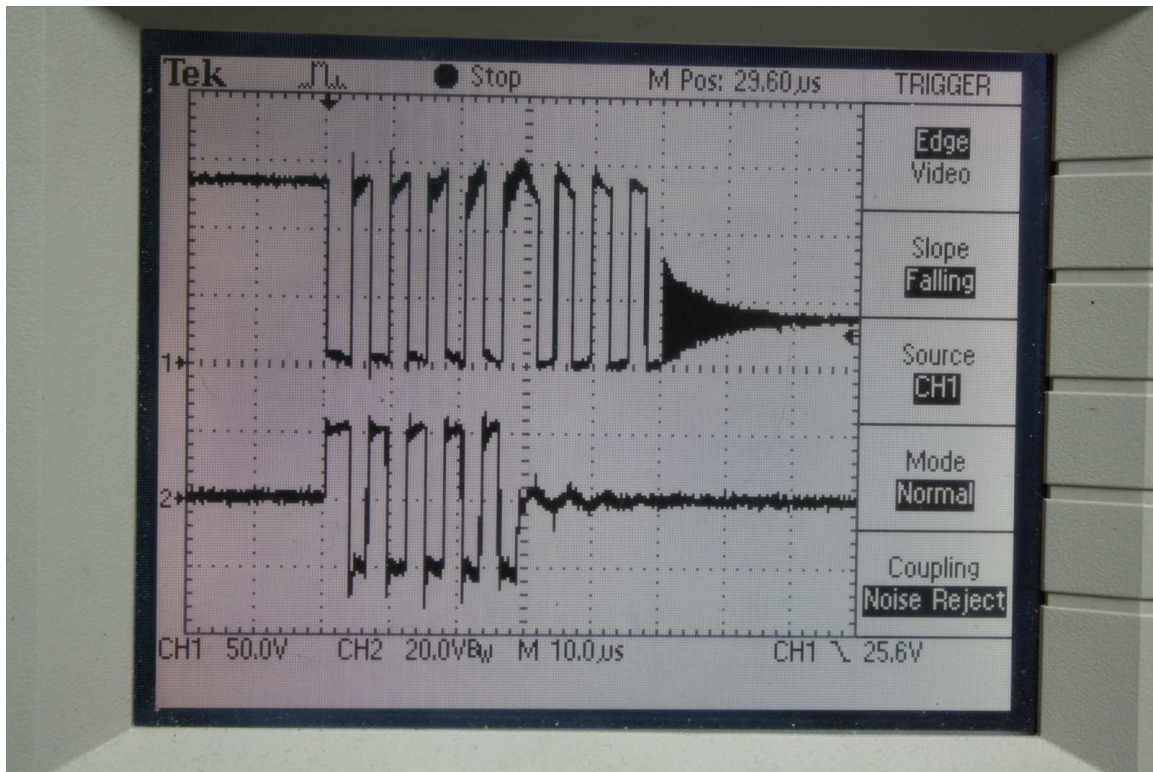
Half bridge output Vs. Gate drive signal. Note the extended first half-cycle, yet there is no significant DC offset on the gate drive waveforms as the GDT supports this OK. Vbus = 30V.
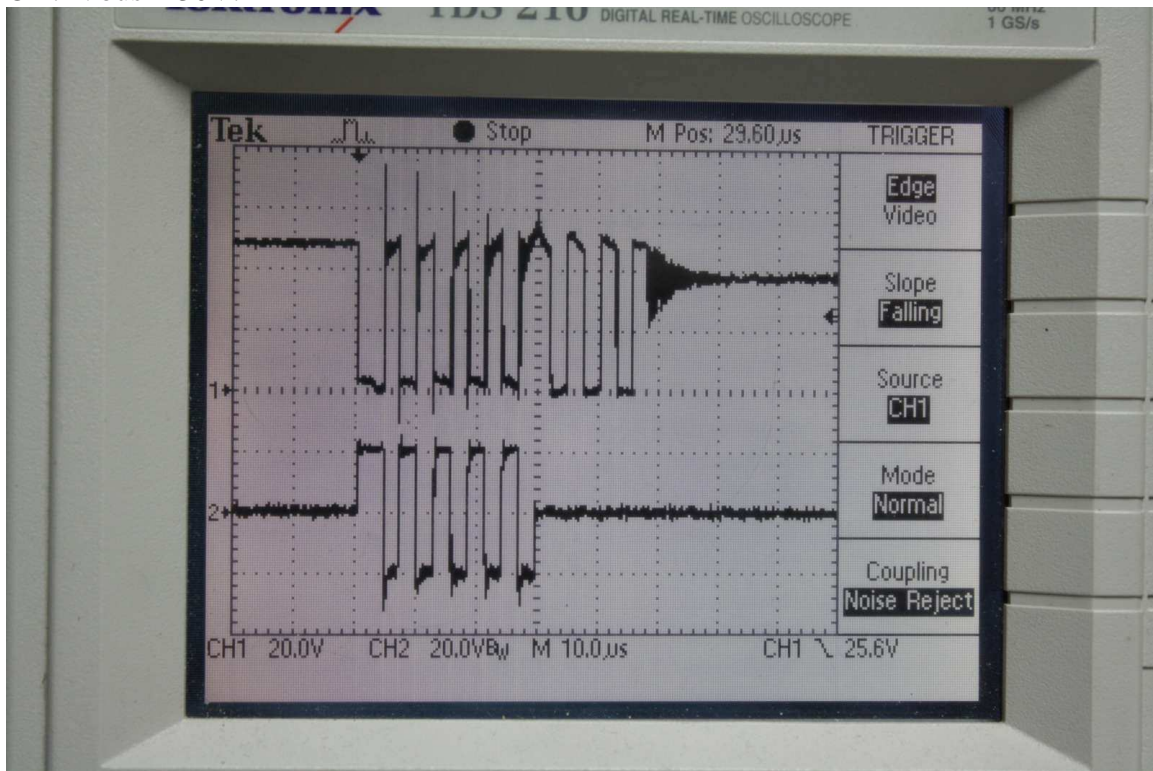
Things start looking better with Vbus nearly 50VDC.

These waveforms look completely acceptable at 140VDC.

A final word about this whole problem and fix: it is mostly an effort to fix any inconsistencies with the drive electronics. I have not had any failures of my DRSSTCs related to the problem, but I have noticed some inconsistency in operation at lower power levels, possibly related to this phenomena.